OIPE JC105
NOV 0 3 2004
PATENT & TRADEMARK OFFICE

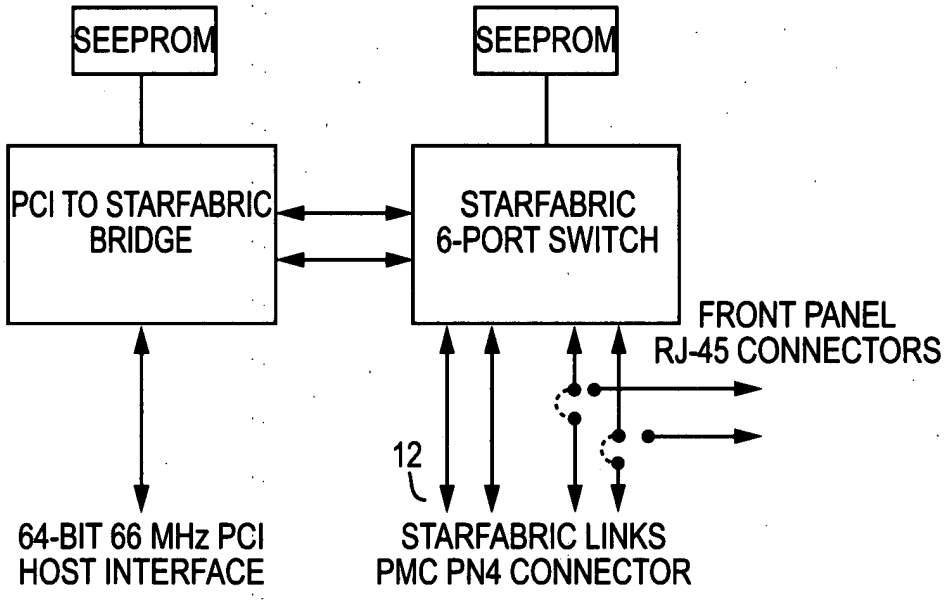

FIG. 1
STARLINK BLOCK DIAGRAM

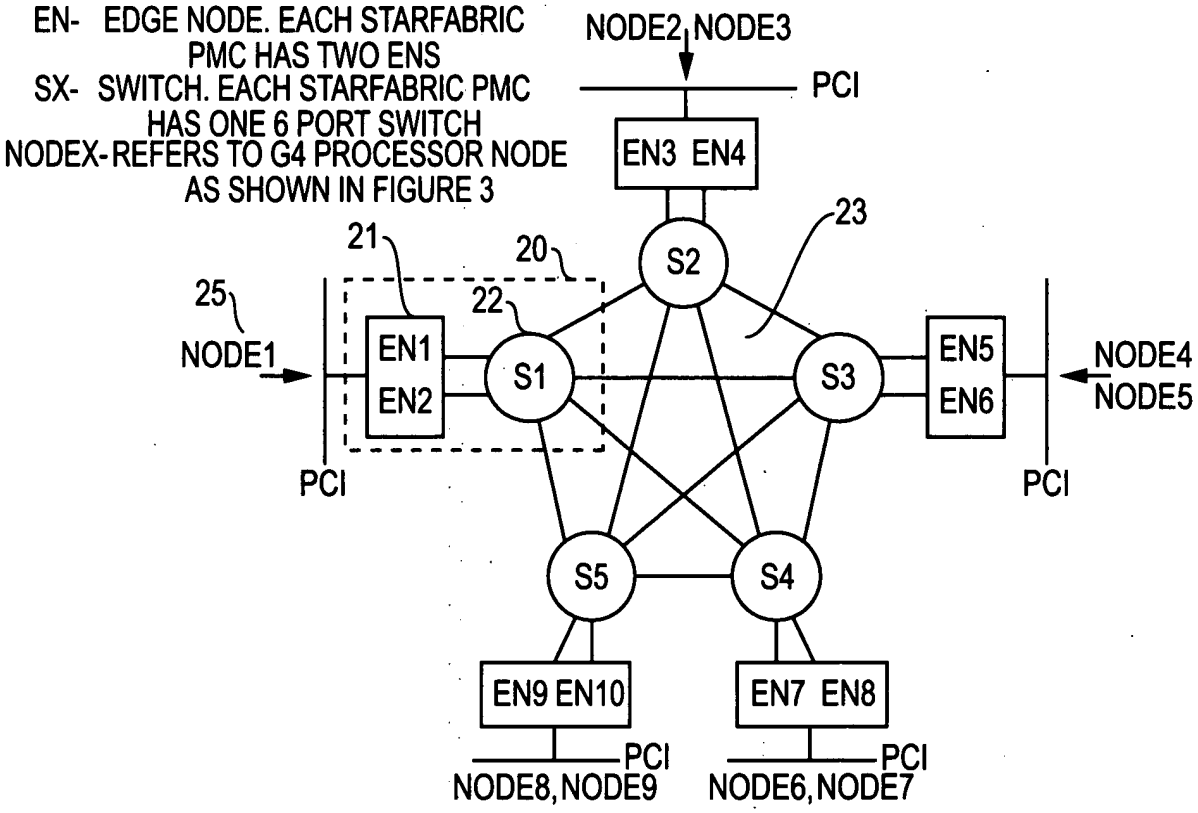

FIG. 2
APPLICATION EXAMPLE:NETWORK TOPOLOGY

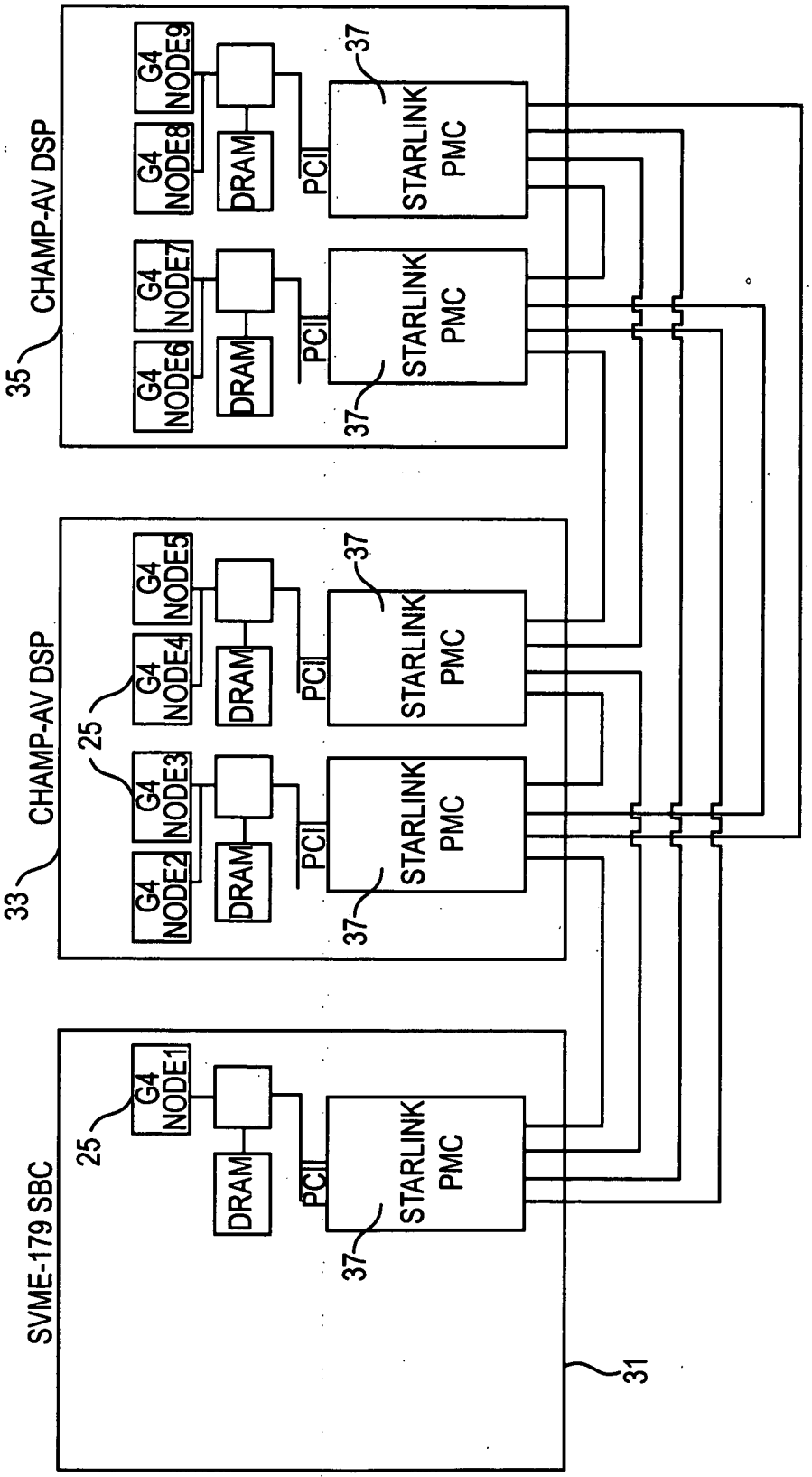

FIG. 3
APPLICATION EXAMPLE: SYSTEM BLOCK DIAGRAM

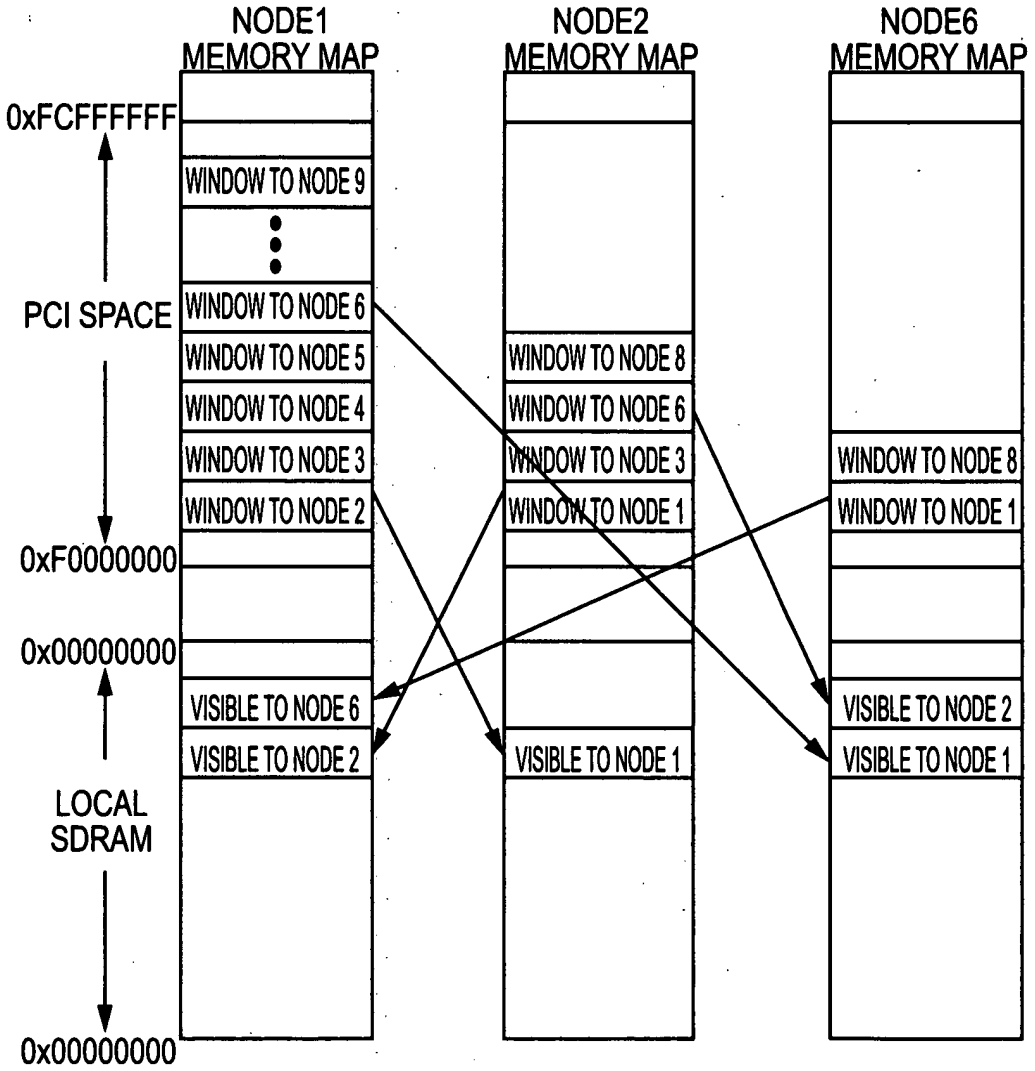

FIG. 4
APPLICATION EXAMPLE:SIMPLIFIED MEMORY MAP

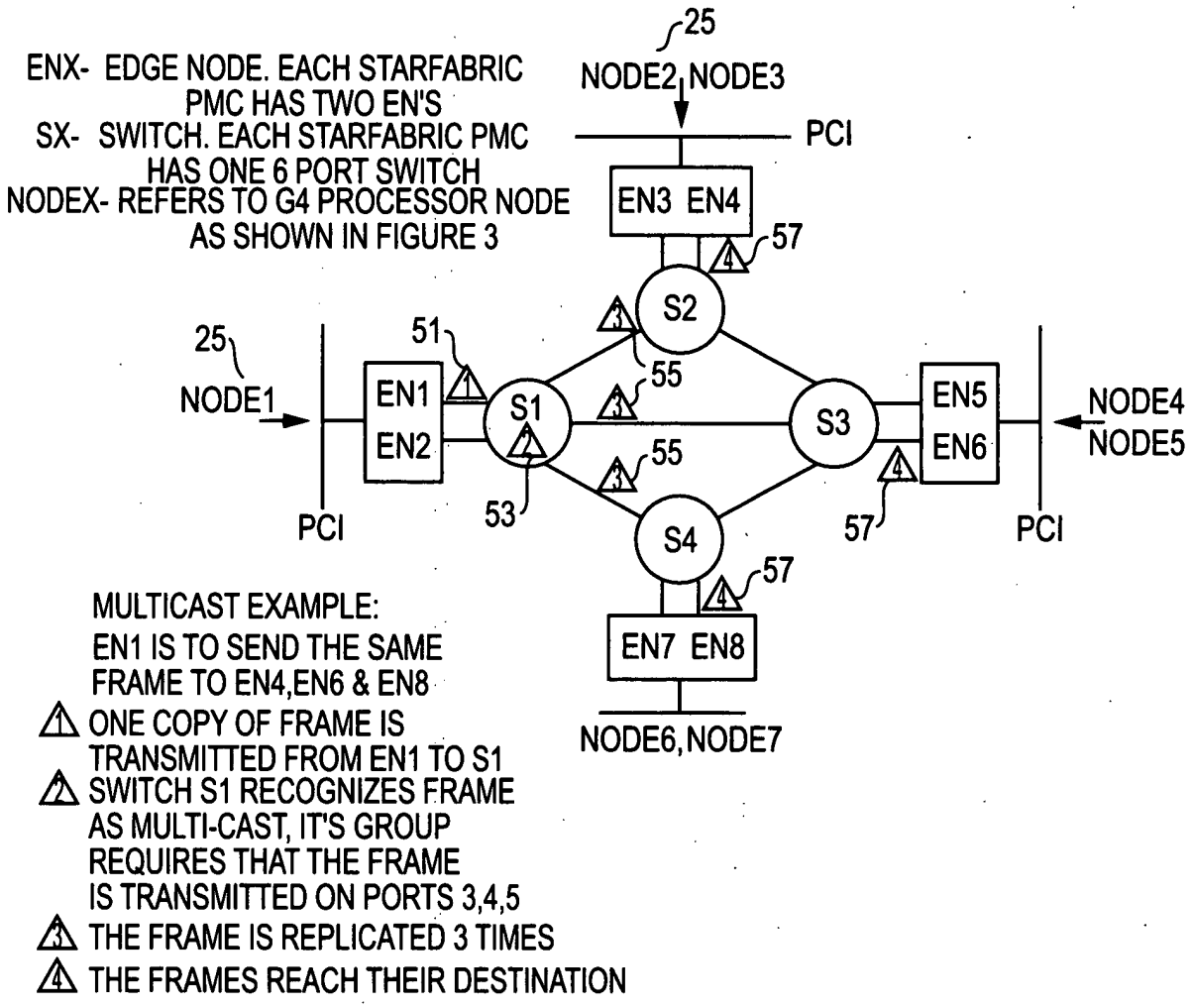

FIG. 5
MULTICAST EXAMPLE

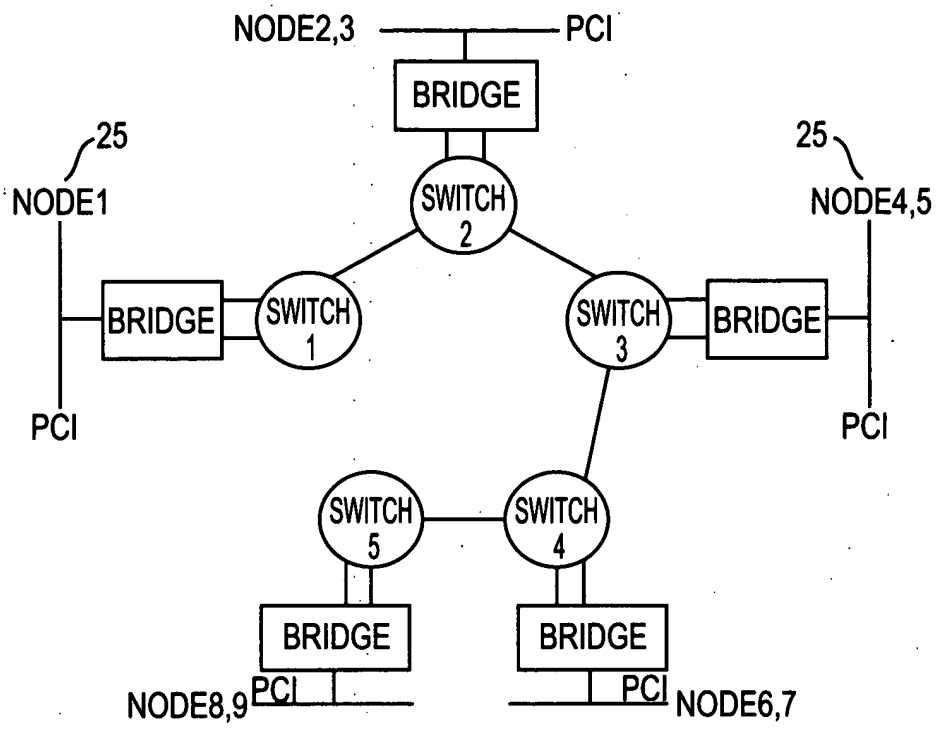
NODE2,3
PCI
BRIDGE
25
NODE1
25
NODE4,5
SWITCH 2
BRIDGE
SWITCH 1
SWITCH 3
BRIDGE
PCI
PCI
SWITCH 5
SWITCH 4
BRIDGE
BRIDGE
NODE8,9
PCI
PCI
NODE6,7

FIG. 6

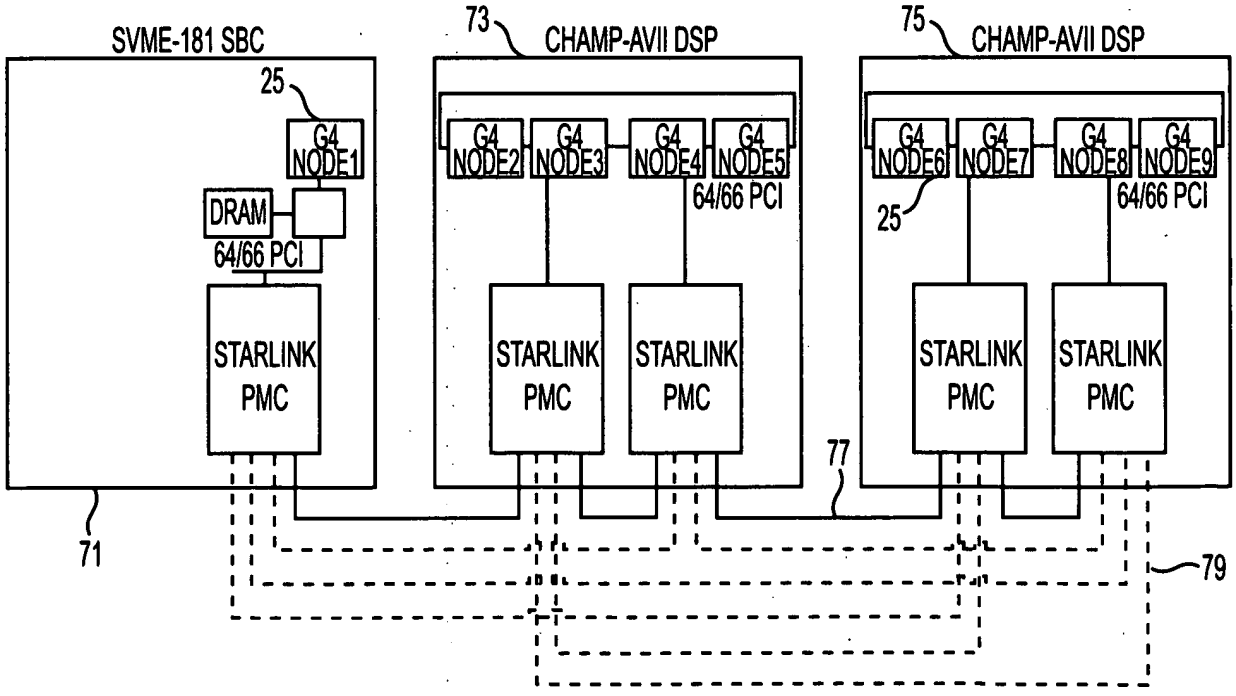
SVME-181 SBC
73
CHAMP-AVII DSP
75
CHAMP-AVII DSP
25
G4 NODE1
DRAM
64/66 PCI
G4 NODE2
G4 NODE3
G4 NODE4
G4 NODE5
64/66 PCI
G4 NODE6
G4 NODE7
G4 NODE8
G4 NODE9
64/66 PCI
25
STARLINK PMC
STARLINK PMC
STARLINK PMC
STARLINK PMC
STARLINK PMC
77
71
79

FIG. 7

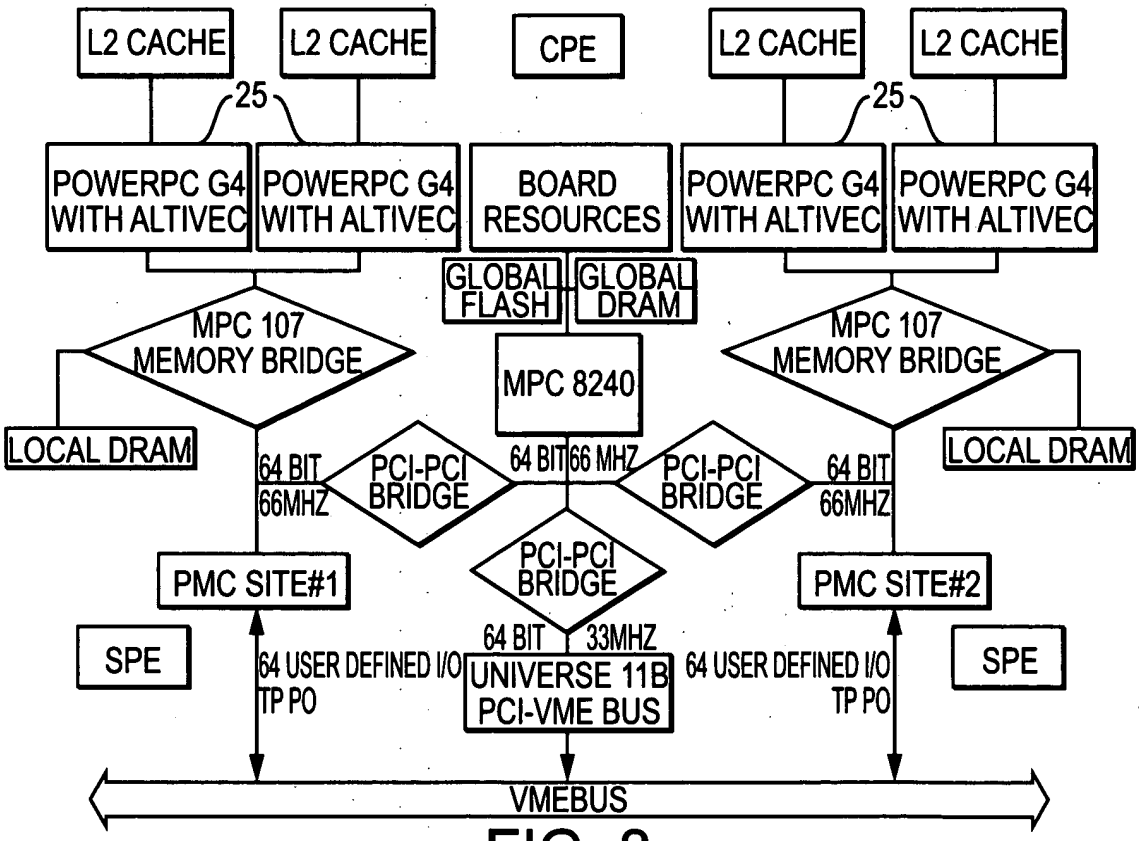
L2 CACHE
L2 CACHE
CPE
L2 CACHE
L2 CACHE
25
25
POWERPC G4 WITH ALTIVEC
POWERPC G4 WITH ALTIVEC
BOARD RESOURCES
POWERPC G4 WITH ALTIVEC
POWERPC G4 WITH ALTIVEC
GLOBAL FLASH
GLOBAL DRAM
MPC 107 MEMORY BRIDGE
MPC 8240
MPC 107 MEMORY BRIDGE
LOCAL DRAM
64 BIT 66MHZ
PCI-PCI BRIDGE
64 BIT 66 MHZ
PCI-PCI BRIDGE
64 BIT 66MHZ
LOCAL DRAM
PCI-PCI BRIDGE
PMC SITE#1
PMC SITE#2
64 BIT 33MHZ
SPE
64 USER DEFINED I/O TP PO
UNIVERSE 11B PCI-VME BUS
64 USER DEFINED I/O TP PO
SPE
VMEBUS

FIG. 8

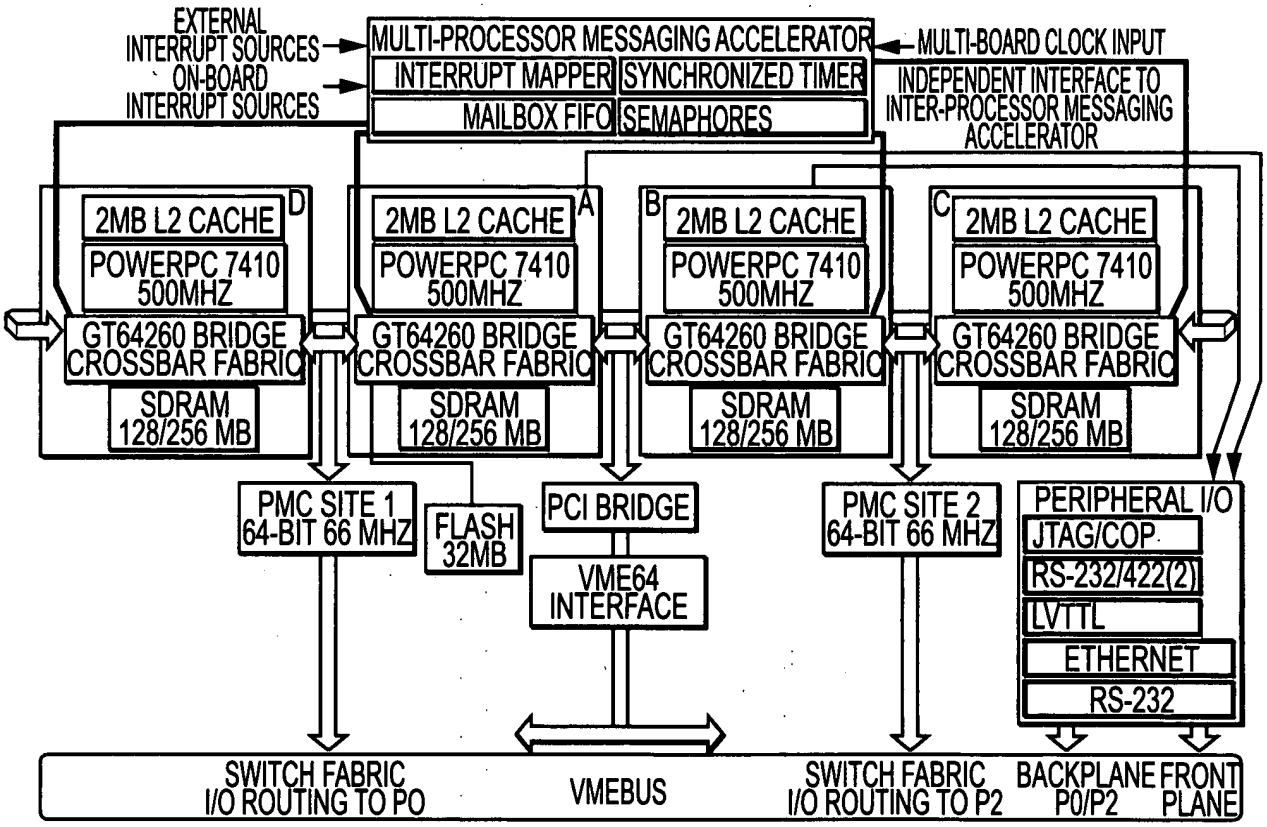
EXTERNAL INTERRUPT SOURCES
ON-BOARD INTERRUPT SOURCES
MULTI-PROCESSOR MESSAGING ACCELERATOR
INTERRUPT MAPPER
SYNCHRONIZED TIMER
MAILBOX FIFO
SEMAPHORES
MULTI-BOARD CLOCK INPUT
INDEPENDENT INTERFACE TO INTER-PROCESSOR MESSAGING ACCELERATOR
D
2MB L2 CACHE
POWERPC 7410 500MHZ
GT64260 BRIDGE CROSSBAR FABRIC
SDRAM 128/256 MB
A
2MB L2 CACHE
POWERPC 7410 500MHZ
GT64260 BRIDGE CROSSBAR FABRIC
SDRAM 128/256 MB
B
2MB L2 CACHE
POWERPC 7410 500MHZ
GT64260 BRIDGE CROSSBAR FABRIC
SDRAM 128/256 MB
C
2MB L2 CACHE
POWERPC 7410 500MHZ
GT64260 BRIDGE CROSSBAR FABRIC
SDRAM 128/256 MB
PMC SITE 1 64-BIT 66 MHZ
FLASH 32MB
PCI BRIDGE
VME64 INTERFACE
PMC SITE 2 64-BIT 66 MHZ
PERIPHERAL I/O
JTAG/COP
RS-232/422(2)
LVTTL
ETHERNET
RS-232
SWITCH FABRIC I/O ROUTING TO PO
VMEBUS
SWITCH FABRIC I/O ROUTING TO P2
BACKPLANE P0/P2
FRONT PLANE

FIG. 9

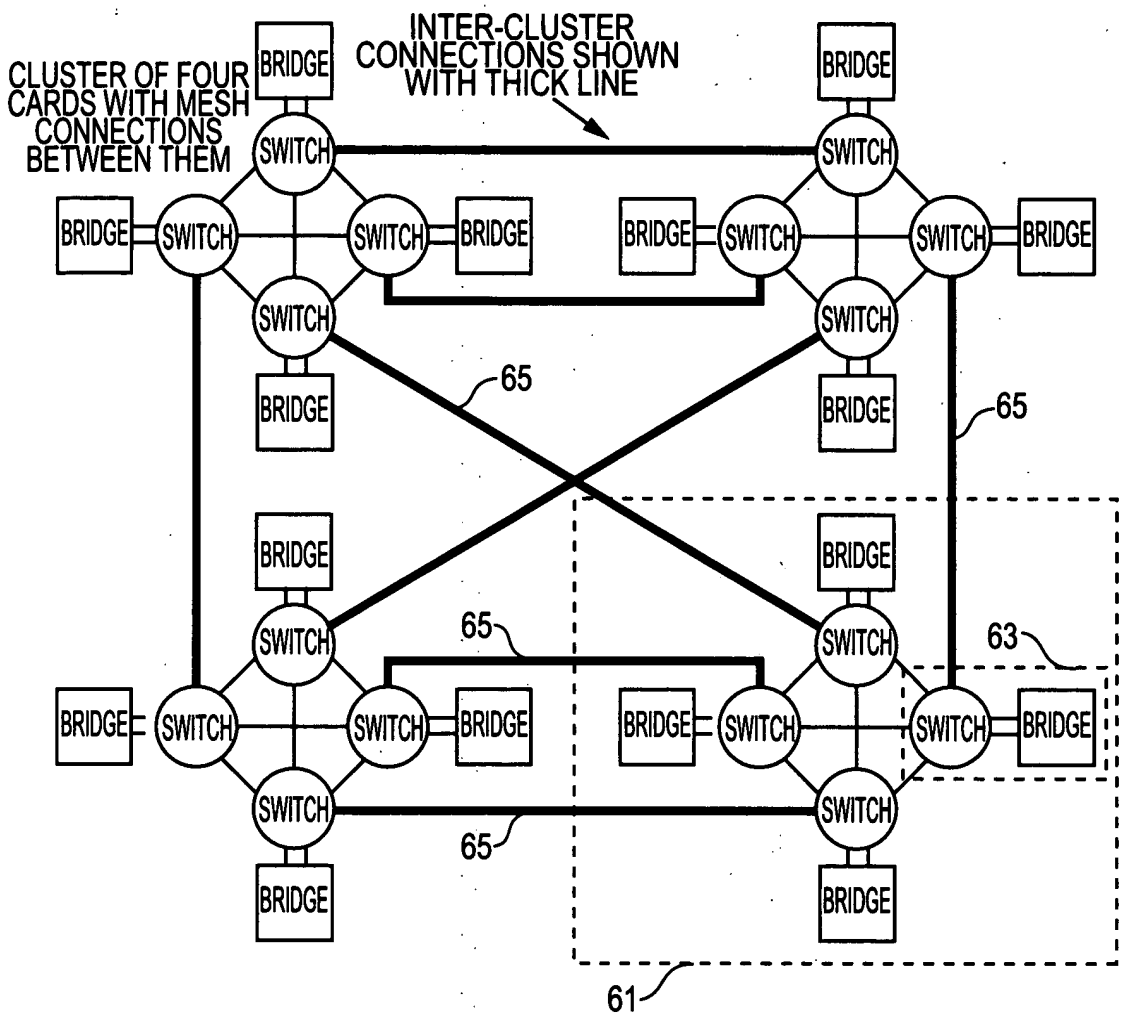
CLUSTER OF FOUR CARDS WITH MESH CONNECTIONS BETWEEN THEM
INTER-CLUSTER CONNECTIONS SHOWN WITH THICK LINE
BRIDGE
SWITCH
65
63
61

FIG. 10